ABSTRACT

Techniques are described for slewing a clock frequency of a clock signal from an initial clock frequency to a final clock frequency. An oscillator provides a number of phase outputs. A current frequency divider value is set to an initial frequency divider value, the initial frequency divider value corresponding to the initial clock frequency. A period of a feedback signal is modified through a number of periods from an initial period to a final period, utilizing one or more of the phase outputs. The current frequency divider value is changed when the period of the feedback signal reaches the final period. The modify and change operations are performed until the current frequency divider value reaches a final frequency divider value, where the final frequency divider value corresponds to the final clock frequency.